LinoSPAD: a time-resolved 256×1 CMOS SPAD line sensor system featuring 64 FPGA-based TDC channels running at up to 8.5 giga-events per second

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ABSTRACT

LinoSPAD is a reconfigurable camera sensor with a 256×1 CMOS SPAD (single-photon avalanche diode) pixel array connected to a low cost Xilinx Spartan 6 FPGA. The LinoSPAD sensor's line of pixels has a pitch of 24 µm and 40% fill factor. The FPGA implements an array of 64 TDCs and histogram engines capable of processing up to 8.5 giga-photons per second.

The LinoSPAD sensor measures 1.68 mm×6.8 mm and each pixel has a direct digital output to connect to the FPGA. The chip is bonded on a carrier PCB to connect to the FPGA motherboard. 64 carry chain based TDCs sampled at 400 MHz can generate a timestamp every 7.5 ns with a mean time resolution below 25 ps per code. The 64 histogram engines provide time-of-arrival histograms covering up to 50 ns. An alternative mode allows the readout of 28 bit timestamps which have a range of up to 4.5 ms.

Since the FPGA TDCs have considerable non-linearity we implemented a correction module capable of increasing histogram linearity at real-time. The TDC array is interfaced to a computer using a super-speed USB3 link to transfer over 150k histograms per second for the 12.5 ns reference period used in our characterization.

After characterization and subsequent programming of the post-processing we measure an instrument response histogram shorter than 100 ps FWHM using a strong laser pulse with 50 ps FWHM. A timing resolution that when combined with the high fill factor makes the sensor well suited for a wide variety of applications from fluorescence lifetime microscopy over Raman spectroscopy to 3D time-of-flight.

Keywords: CMOS, SPADs, FPGA, TDC, single-photon avalanche diodes, image sensor, reconfigurability, time-of-flight, 3D imaging

1. INTRODUCTION

Since the 1960s avalanche photodiodes (APDs) and later Single-photon avalanche diodes (SPADs) enable the detection of light at the highest sensitivity: that of a single photon. Numerous publications cover the history from the first APDs to the modern day SPADs.[1,2]

As the manufacturing processes for consumer micro-electronics matured it became possible to integrate SPADs alongside electronic circuits on a single CMOS substrate. Shortly afterwards the first SPAD arrays were implemented[3] and mass-production of SPADs in standard CMOS technology is today established.[4]

The reliable fabrication of SPADs in standard CMOS requires a mature process in terms of cleanliness which is directly related to dark count rate as the voltage above the breakdown cannot be sustained for long periods in the presence of defects. The operating conditions of SPAD circuits are generally outside normal conditions for digital electronics and often not specified by manufacturers. This leads to additional research being necessary before larger SPAD circuits can be successfully implemented in a new process.

A SPAD amplifies the charge generated upon the arrival of a photon to a macroscopic voltage that triggers digital processing circuitry. Simpler circuits count the number of photons arriving in a time window, while more

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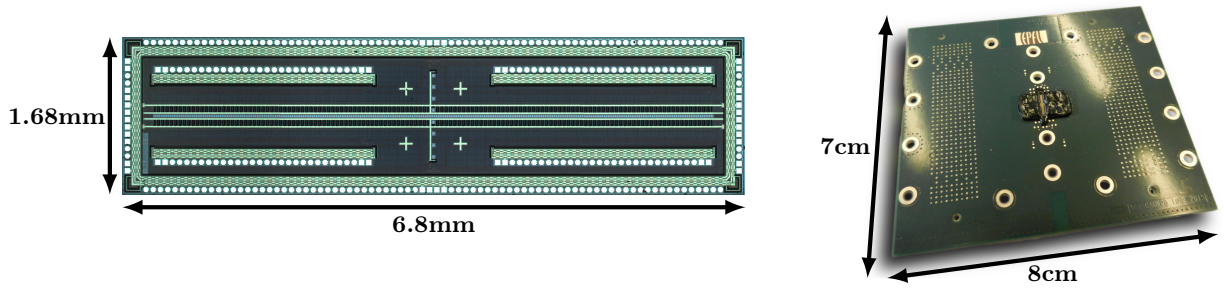


(a) (b)

Figure 1: (a) Micrograph of the SPAD line sensor with clearly visible alignment marks and auxiliary vertical line of pixels. (b) PCB carrier with the sensor bonded to it.

complex circuits can timestamp individual photons. More and more applications make use of this capability. The category of time-correlated single-photon counting (TCSPC[5]) covers many such applications, among them fluorescence lifetime microscopy (FLIM) and similar methods in the field of biology.[6]

Instead of integrating more functionality inside the sensor chip itself we chose a radically different approach for the camera system we present in this paper. A line of SPAD pixels with a good fill factor and low noise implemented in a 0.35 µm CMOS process is connected directly to a FPGA. This gives us maximum flexibility in photon processing and allows quick evaluations of possible future processing circuitry to be fabricated in advanced technologies.

We present the camera design starting with the SPAD sensor in section 2 followed by the FPGA firmware in section 3. The sensor and TDC performance is presented in section 4 before their application in a 3D-time-of-flight imaging setup shown in section 5.

2. SPAD LINE SENSOR

The SPAD sensor used in our camera has been produced in a standard 0.35 µm high-voltage CMOS process. The pixel diodes have a pitch of 24 µm and an active area in the form of a square with rounded corners that covers approximately 40% of the area. They are implemented using a deep n-well for the cathode below a p+ type anode. A p-well guard ring is used to prevent premature edge breakdown.

Each diode has a quenching transistor and a two-stage CMOS inverter next to it to drive the output buffers. To accommodate output buffers for each pixel without making the sensor die prohibitively large a staggered layout is used for the 312 bonding pads. 192 pads are on the periphery of the chip while the remaining 120 pads are distributed to 4 blocks inside the chip. The chip is directly bonded to a carrier PCB with high-density connectors to connect to the FPGA board.

Figure 1a shows the micrograph of the chip with alignment crosses and 8 auxiliary pixels also usable for alignment. Figure 1b shows the 8 cm×7 cm carrier board for the sensor.

Comparable CMOS SPAD line sensors with TDCs integrated on the sensor die have been presented recently.[7,8] They target Raman spectroscopy and fluorescence spectroscopy respectively and are optimized for these applications. Their TDCs do not reach the resolution of the FPGA solution presented here and hence demonstrate that high timing resolution is not always necessary for practical applications.

3. FPGA

The Spartan 6 FPGA connects directly to the outputs of the 256 SPAD pixels and implements 64 time-to-digital converters (TDCs) to timestamp photon arrivals. The high level firmware architecture is shown in Figure 2. A computer communicates with the camera over USB to configure acquisition and post-processing settings before requesting it to measure photon events and send histograms of photon arrival times.

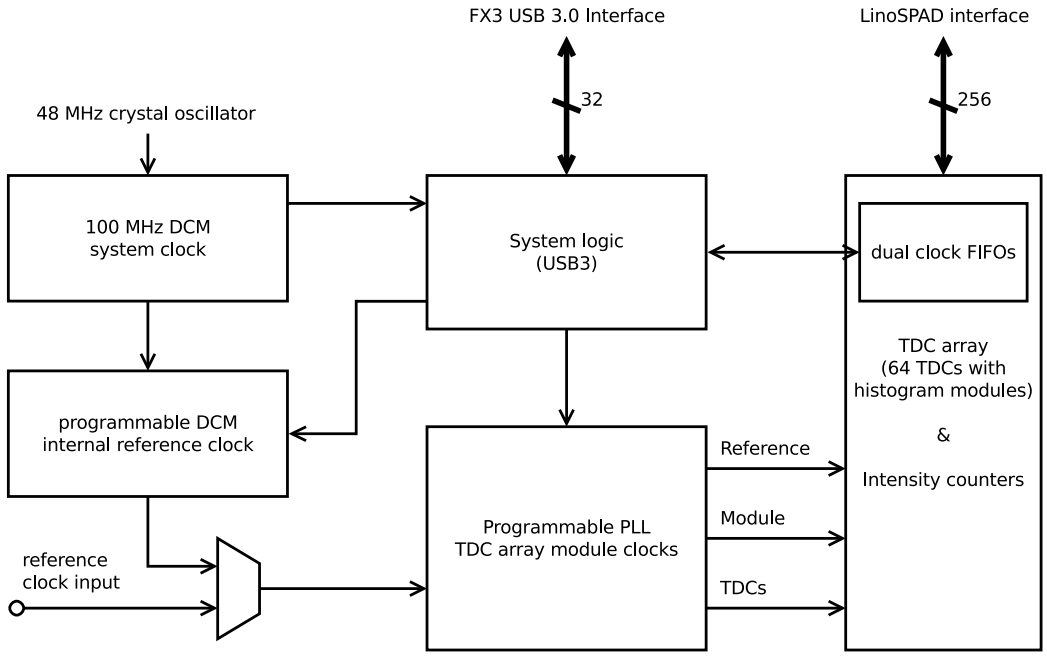


Figure 2: High level block diagram of the FPGA firmware. The FPGA receives configuration and acquisition commands over USB to program the clocks for synchronous acquisitions and sends histogram data to the computer as requested.

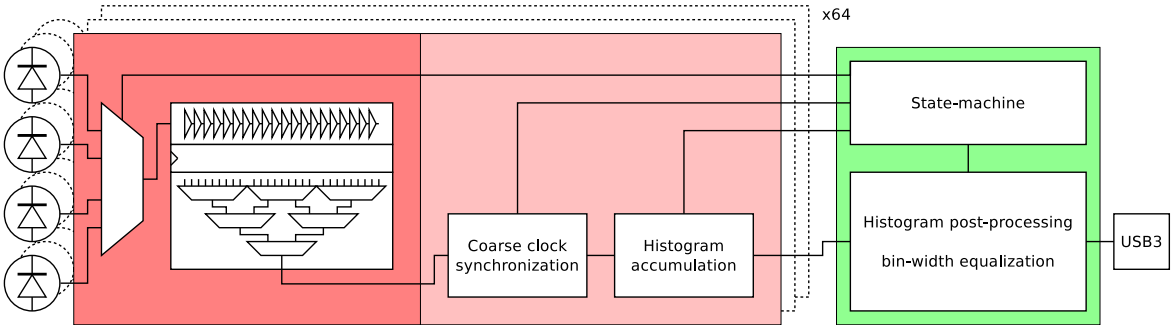


Figure 3: Data flow diagram from SPAD events to histograms. The dark red part is running at 400 MHz, the other parts at 133 MHz. The red front-end is replicated 64 times while the green state-machine and post-processing is shared between the TDC modules.

Figure 3 details the main processing pipeline from the event detection through the histogram engine and post-processing to the computer. We describe the different blocks from the pixel to the computer.

Since 4 pixels share a TDC there is a multiplexer allowing only one pixel at a time to trigger the delay line. This is to prevent ambiguity concerning the source of the event. Through the multiplexer the selected pixel is connected to a carry chain delay line sampled at 400 MHz. The length of the chain is 35 carry elements for 140 bits, long enough to cover the 2.5 ns period with sufficient margin for varying placements and operating conditions inside the FPGA.

Samples from the delay line go through a thermometer-to-binary encoder also running at 400 MHz before the frequency is reduced to 133 MHz. This reduction in frequency is done by looking at three samples and eventually retaining one corresponding to a photon event. At this point the delay line sample has been converted to a 9-bit value between zero and 420 covering a 3×2.5 ns wide window of the arrival time.

A programmable reference circuit allows the synchronization of the TDC modules with external sources

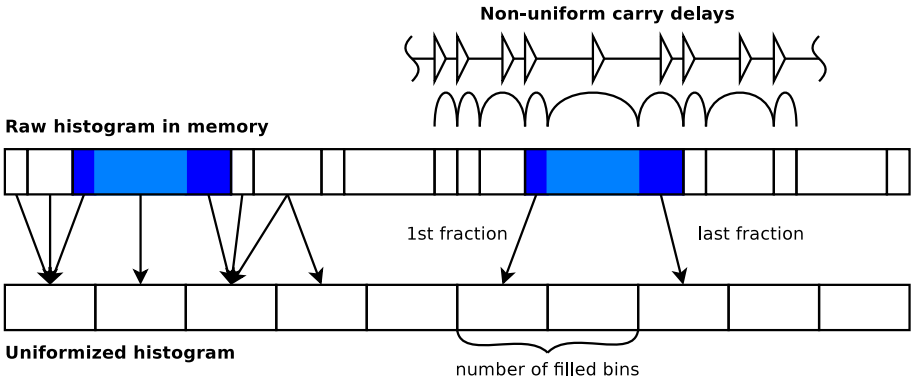


Figure 4: Illustration of the histogram processing algorithm. Input bins of different sizes are remapped to output bins of uniform size. The blue example shows a large input bin being split across three smaller output bins by defining the fractions to be split off and the number of bins to complete.

Table 1: FPGA TDC comparison.

	This work	Favi[9]	Fishburn[10]	CERN[11]
FPGA	Spartan 6	Virtex 5	Virtex 6	Spartan 6
Process [nm]	45	65	40	45
Number of TDCs	64	1	160	2
Resolution [ps]	25	17	10	26
Event rate [MHz]	133	300	300	125
Carry blocks [/TDC]	35	50	40	124
Clock frequency [MHz]	400	300	600	125

running at frequencies from a few kHz up to 100 MHz with the FPGA providing a reference clock or locking its PLL onto a provided one. This reference has to be synchronized with the sampling and processing clock.

The blocks following the encoder receive the fine value and locate it within the longer time-frame given from the reference before passing it to the histogram memory module for accumulation. When the accumulation period is finished, a read-out is triggered and the memory modules of each TDC pass their data one after another through the post-processing to the USB engine. The memory module is double buffered such that accumulation can continue on the next pixel during the readout period.

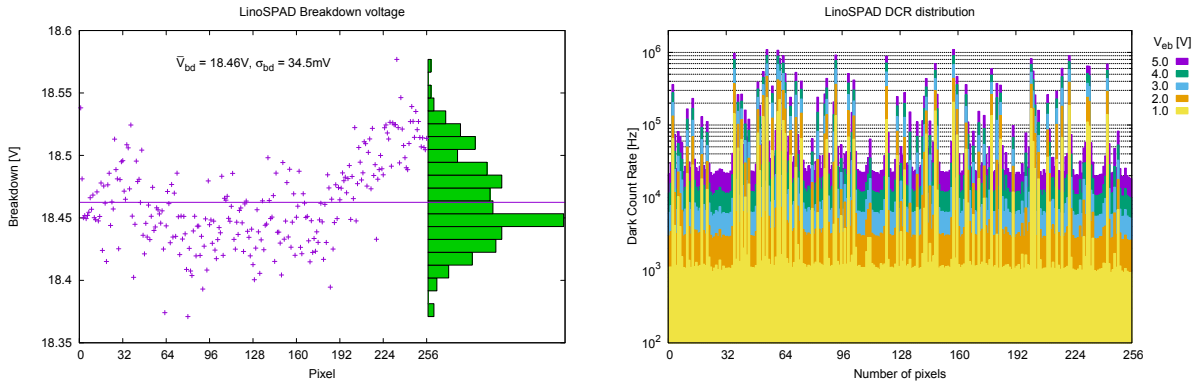
The readout happens at a rate of 32 bits per cycle at 100 MHz, the maximum speed of the USB link present on the camera. During the readout the arrival time histograms can be processed to remove non-linearities from the FPGA delay lines. Figure 4 illustrates the correction algorithm used whereby a raw bin is summed into one or split across processed bins. During this post-processing no events are artificially created or destroyed. Rather the counts in the raw histogram are redistributed in the processed histogram to create a uniform count density.

With 64 TDCs our FPGA firmware is capable of continuously accumulating histograms at up to 8.5 giga-events per second covering reference periods up to 50 ns with a resolution better than 100 ps.

Other FPGA based TDCs have been proposed with varying trade-offs regarding the number of channels, timing resolution and timing range. Table 1 lists a few designs based on Xilinx FPGAs.

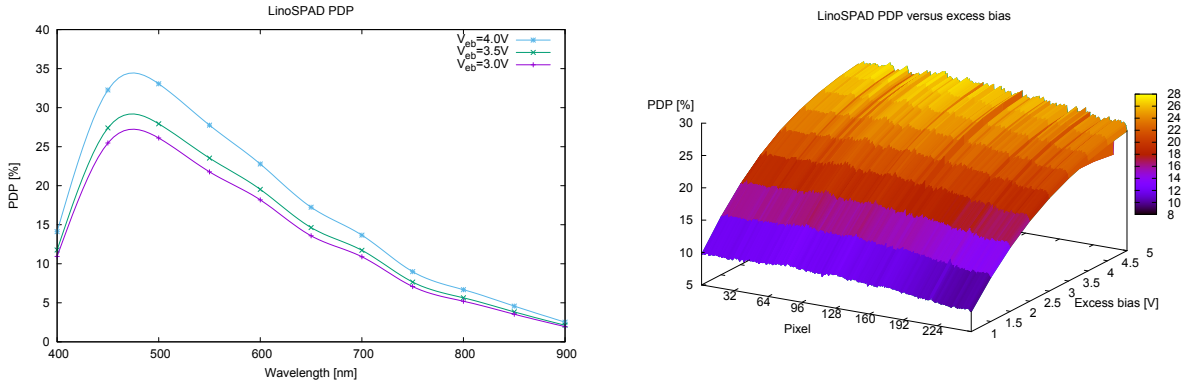
4. PERFORMANCE EVALUATION

Using intensity counters inside the FPGA we evaluated the main characteristics of our SPAD sensors, namely the breakdown voltage, the dark count rate and the photon detection probability. We show here value from a typical chip.



(a) (b)

Figure 5: (a) Breakdown voltage over the SPAD line. (b) DCR distribution over the line for excess voltages from 1V to 5V.



(a) (b)

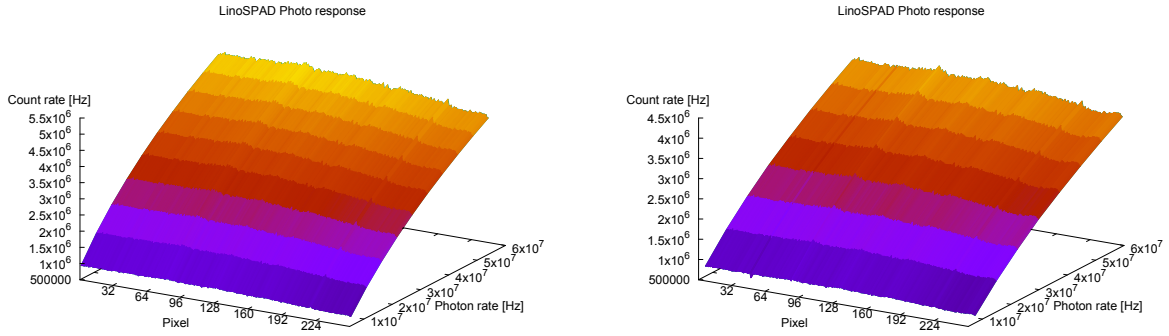
Figure 6: (a) Photon detection probability versus wavelength for a typical pixel. (b) Photon detection probability at 465 nm per pixel for excess bias voltages from 1V to 5V. The noisiest pixels reach saturation for higher voltages.

In Figure 5a we show the estimated breakdown voltage across the line of SPADs. In the chip shown here we see a clear rising trend of the breakdown voltage towards one end of the line. This has been observed in multiple, but not all chips tested so far. Still the standard deviation of the breakdown voltage is typically around 35 mV. The breakdown voltage was estimated using a fit-to-DCR where we fitted a two-piece linear function to the DCR values and use the position of the knee as effective breakdown voltage. From this voltage we subtract 0.6 V for the output inverter threshold.

After measuring the breakdown voltage we measured the noise of the sensor expressed in the dark count rate (DCR), the rate of avalanche events without photons impinging the sensor. Figure 5b shows the DCR distribution over the line for excess bias voltages up to 5V above breakdown. About 25% of the pixels exhibit a DCR significantly over the median value which is mostly due to the square shape of the SPADs which are more prone to high noise than round diodes.

Also measured was the typical photon detection probability for wavelengths between 400 nm and 900 nm as shown in Figure 6a and per-pixel photon detection probability shown in figure 6b for 465 nm. Figure 7 shows the photo response at 465 nm and 640 nm for a fixed excess bias of 2V at increasing illumination levels.

The TDC performance was characterized from uncorrected arrival time histograms over a period of 12.5 ns. Using a constant current driven LED source to illuminate the chip the arrival times of photons should be uniformly distributed in time. By analysing the distribution of our measured histograms we can thus estimate the real bin sizes of our TDCs which can have large non-linearities. These non-linearities are caused by the

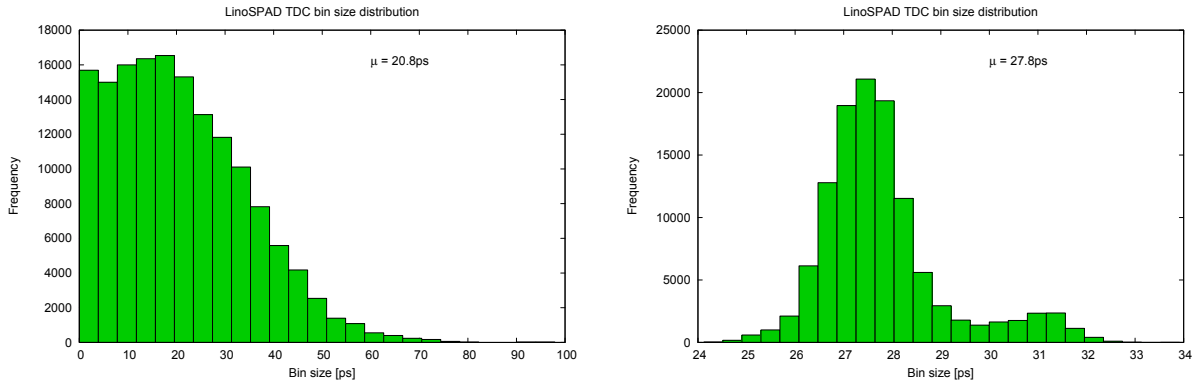


(a) (b)

Figure 7: Photoresponse at 465 nm (a) and 640 nm (b) for a fixed excess bias of 2V and illumination levels from 1 μW/cm^2 to 10 μW/cm^2.

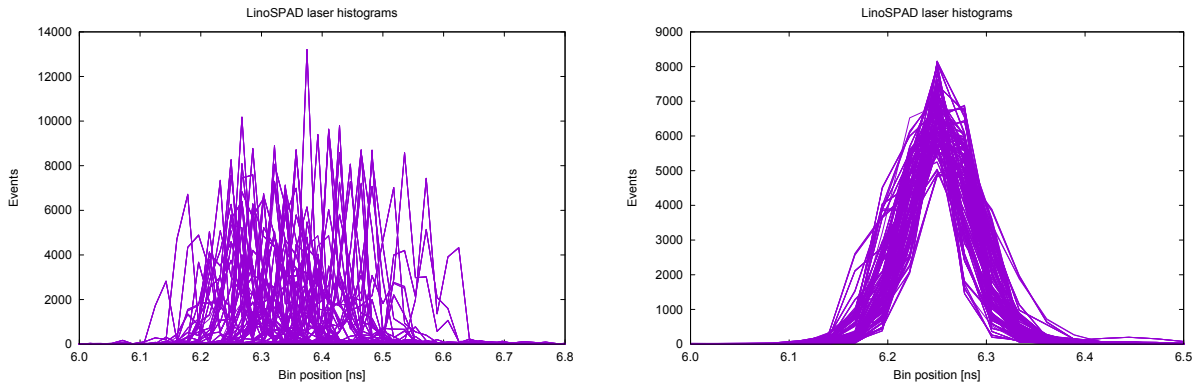
Table 2: LinoSPAD performance data.

Chip size	6.8 ×1.68 mm^2
Technology	AMS HV 0.35µm 4M
Resolution	256 ×1 (+8)
Pixel pitch	24 µm
Fill factor	40%
Dead time	<100 ns
Median DCR @ 20°C	2.5 kHz
Spectral range (PDP > 5% @ 3V$_{eb}$)	400-850 nm
Light incidence	45° from normal
Number of TDCs	64
Maximum TDC event rate	133 MHz/TDC
Average TDC resolution	<25 ps
TDC range	28 bit (4.5 ms)
Histogram rate	150 k/s (>200 MB/s)



(a) (b)

Figure 8: (a) Estimated time bin sizes over all TDCs from illumination with a 640 nm LED. Only bins that contain events are counted. (b) Apparent bin sizes after correction to have 450 uniform bins for a 12.5 ns period.



(a) (b)

Figure 9: Arrival time histograms from illumination with a synchronized pulse laser without (a) and with (b) post-processing. With an illumination intensity of 4 μW/cm^2 this is effectively a measure of the camera instrument response function. The measured FWHM for processed histograms is below 100 ps.

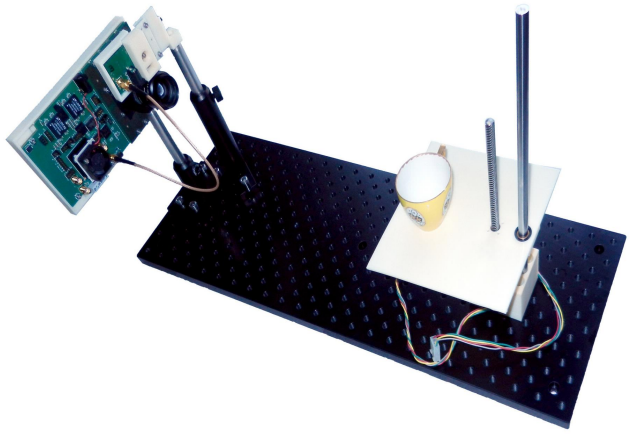


Figure 10: Setup for the 3D-scan of the cup. Over the camera objective is the pulsed laser diode used for illumination. The scan stage was constructed using a stepper motor connected to a drive screw.

physical implementation of the carry chains in the FPGA that are used to delay our signal while getting the highest possible time precision.

Our encoder after the delay line forces the timestamps to be monotonous and a sample covering 2.5 ns uses always a block of 140 codes. By looking at the timestamp distribution in a 2.5 ns period we can thus infer the effective time span for each possible timestamp and afterwards program our post-processing module to create a uniform histogram. Figure 8 shows the distribution of timestamp bin sizes captured by the TDCs before and after post-processing.

After post-processing we reach a very low non-linearity as shown in Figure 9 where the histograms of all pixels are overlaid. The average FWHM with a strong laser pulse signal is below 100 ps for the processed histograms.

Table 2 summarizes the characteristics of our camera system.

5. 3D TIME-OF-FLIGHT IMAGING

Having an accurate photon time-of-flight sensor it seemed natural to us to build a 3D camera. There are two main difficulties to overcome to build a 3D camera with our system. The first is the illumination system, the second is imaging an area onto a line sensor. For our test-setup we chose to illuminate the whole scene from a laser diode driven by a custom pulse circuit synchronized with the camera and to build a vertically translating stage to move an object to be imaged in front of the camera. We are well aware, that our setup is not optimal regarding photon efficiency scanning accuracy.

Figure 10 shows the scanning setup used to acquire 3D time-of-flight data. Instead of moving the object in front of the camera, the camera could be moved. In an optimized system with a minimum of moving parts there would only be an oscillating mirror in front of the camera. The illumination part can be optimized by restricting the illumination to the line that is currently being scanned. Focussing the light on one line has the added advantage of a better signal-to-noise ratio or makes it possible to use higher intensities. For a first demonstration of our system and to evaluate the 3D time-of-flight performance of our camera however, these optimizations were of lesser importance and are not further examined here.

In Figure 11 we show the result of a scan of a small cup approximately 55 mm wide at the top and 45 mm tall. The cup is illuminated by a 660 nm laser diode (Opnext HL6545MG) driven from the camera with a pulse rate of 66 MHz. The cup at a distance of approximately 35 cm is imaged through a 25 mm objective (Thorlabs MVL25M23) on the line sensor. At each line we capture an arrival time histogram over 45 ms (approx. 3M pulses) and show the position of maximum intensity after FPGA-processing.

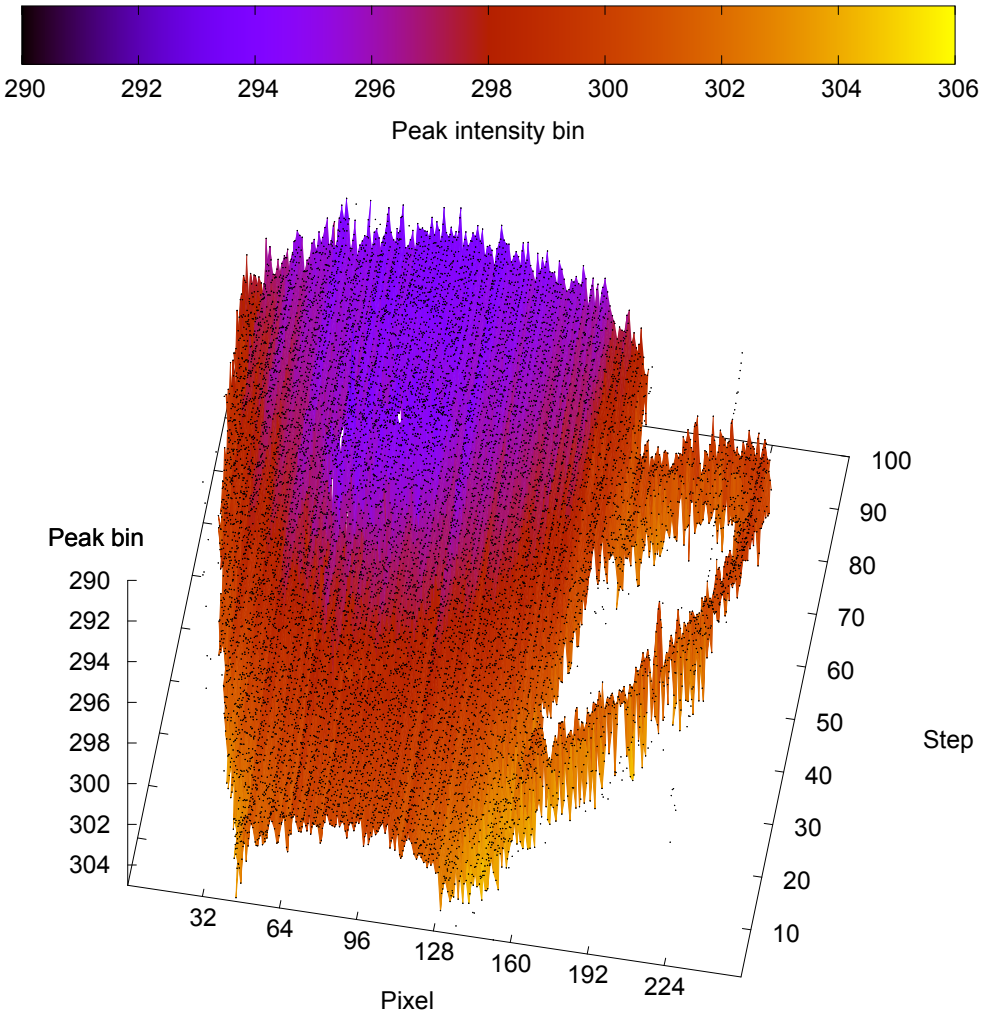


Figure 11: Line scan of a cup using 100 histograms of 45 ms. The depth information shown is the position of the position of maximum intensity in a FPGA-processed histogram of 600 bins for 15 ns. (25 ps/code)

6. CONCLUSION

We have demonstrated a reconfigurable camera based on a simple SPAD line sensor coupled with a low-cost FPGA. On the FPGA we implemented 64 TDC modules, each capable of accumulating histograms at an event rate of up to 133 million events per second. Post-processing in the FPGA reduces the inherent non-linearities of FPGA delay lines to obtain a time resolution below 100 ps FWHM, a time resolution sufficient for a large number of applications.

Before demonstrating the ability to rapidly acquire time-of-flight 3D images we evaluated the basic characteristics of the SPAD line sensor in terms of breakdown voltage, dark count rate and photon detection efficiency. We show a high uniformity across the pixels in terms of photo response. The FPGA TDCs are evaluated by analysing the inherent non-uniformity of the delay lines built from dedicated carry lines and we show how to account for this non-uniformity in real-time.

By synchronizing our TDCs with a pulsed laser illumination we are able to acquire time-of-flight histograms from the SPAD pixels at high rates. In combination with a mechanical scanning system we build a small 3D-scanner to illustrate the combined capabilities of our camera.

The high time resolution combined with the reconfigurable processing capabilities of an FPGA make the system well suited to build prototypes of time-correlated single-photon counting (TCSPC) systems and evaluate possible novel applications.

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