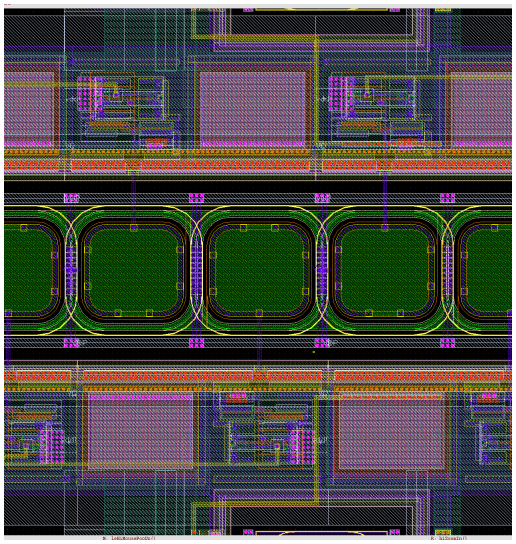
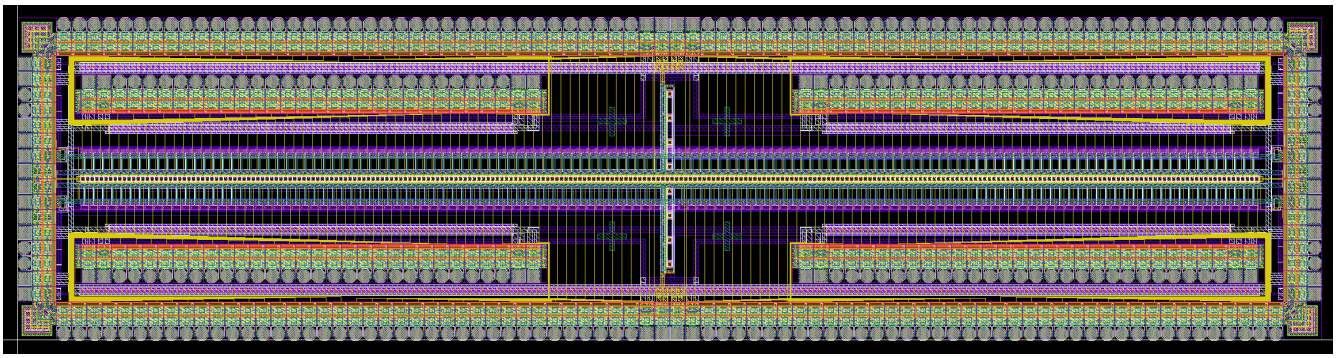
LinoSPAD Camera Factsheet

Sensor specification:

Chip size:	6.8 x 1.68 mm²
Technology:	AMS HV 0.35um 4M
Resolution:	256 x 1 (+8)
Pixel pitch:	24 um
Sensitive area diameter:	~17.3 um
Fill factor:	~41%
Dead time:	Est. 100 ns
Median DCR @ 25°C:	~2.5 kHz
Target wavelength:	400-850 nm
Light incidence:	< 45° from normal



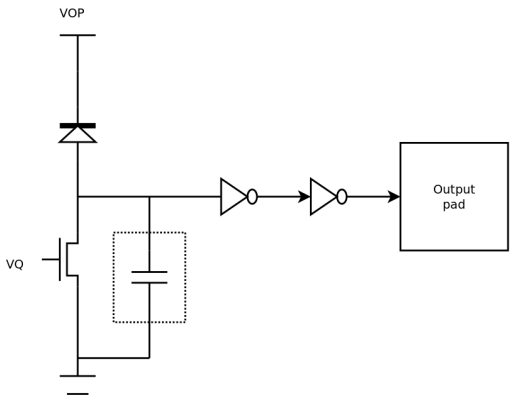
Close-up of SPADs



Full layout

LinoSPAD is a simple sensor with a line of SPADs implemented in a standard high-voltage CMOS process. (AMS 0.35um)

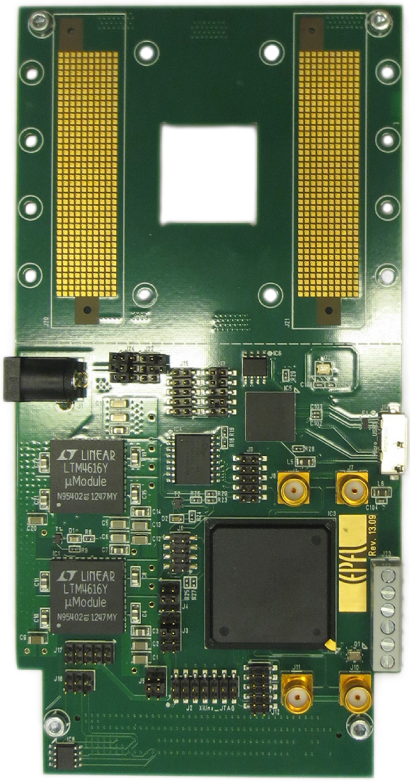
The chip size is 6.8 x 1.68 mm² and there are 256 SPADs with a pitch of 24um. A total of eight alignment markers are distributed around the center of symmetry of the chip. There is a secondary line of 8 detectors with a pitch of 127um vertically. The SPADs are rounded rectangles with an approximate fill factor of 41% in the line. All SPADs connect directly to outputs as seen in the pixel schematic.



Pixel schematic

Camera mainboard:

FPGA:	Xilinx Spartan 6 LX 150 (FGG676)
Interfaces:	• Standard Xilinx JTAG • Cypress FX3 USB 3.0 transceiver (tested over 250 MB/s between FPGA and PC)
Memories:	• S25FL128S 128 Mbit SPI flash for FPGA configuration (Xilinx Impact supported) • M25P16 SPI flash for FX3 configuration
Power:	5V main power input, two dual 8A regulators for 1.2V, 1.8V, 2.5V and 3.3V on board. FPGA I/O voltages jumper selectable.
FPGA Clocks:	48 MHz oscillator and 100 MHz clock from FX3. 2 SMA on 2.5V I/O and 2 on 1.8V – 3.3V I/O. (Differential input possible.)
Extension:	FMC daughter card connector on the back to connect to other Xilinx FPGA boards.
Sensor I/O:	296 FPGA I/O and 4 voltages on two SAMTEC GFZ 40x10 connector arrays. I/O voltage selectable between 1.8V and 3.3V. Three voltages brought out two screw terminal.



Camera mainboard

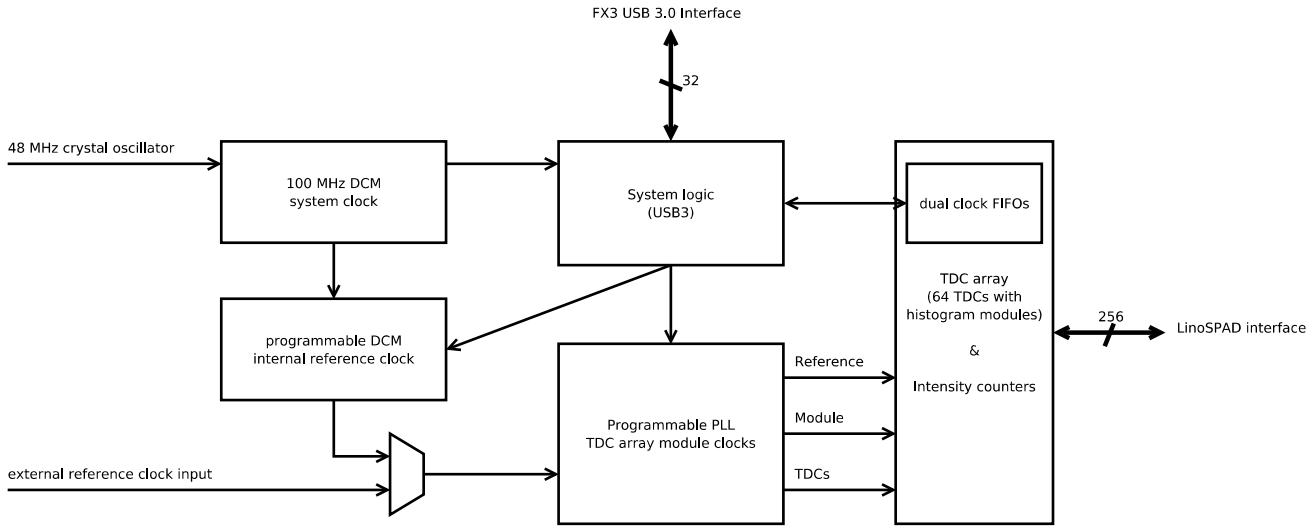
Standard firmware:

The FX3 USB 3.0 transceiver is used as transparent FIFO between the computer and the FPGA. Transfer speeds over 250 MB/s are reached with the current firmware-software combination.

The FPGA firmware as shown in the schematic below implements 64 TDCs with histogram modules that are assigned to the pixels in time-division multiplexing mode. (A version with opportunistic concurrent acquisition is in development.) Intensity counters are connected in parallel and always active on all pixels.

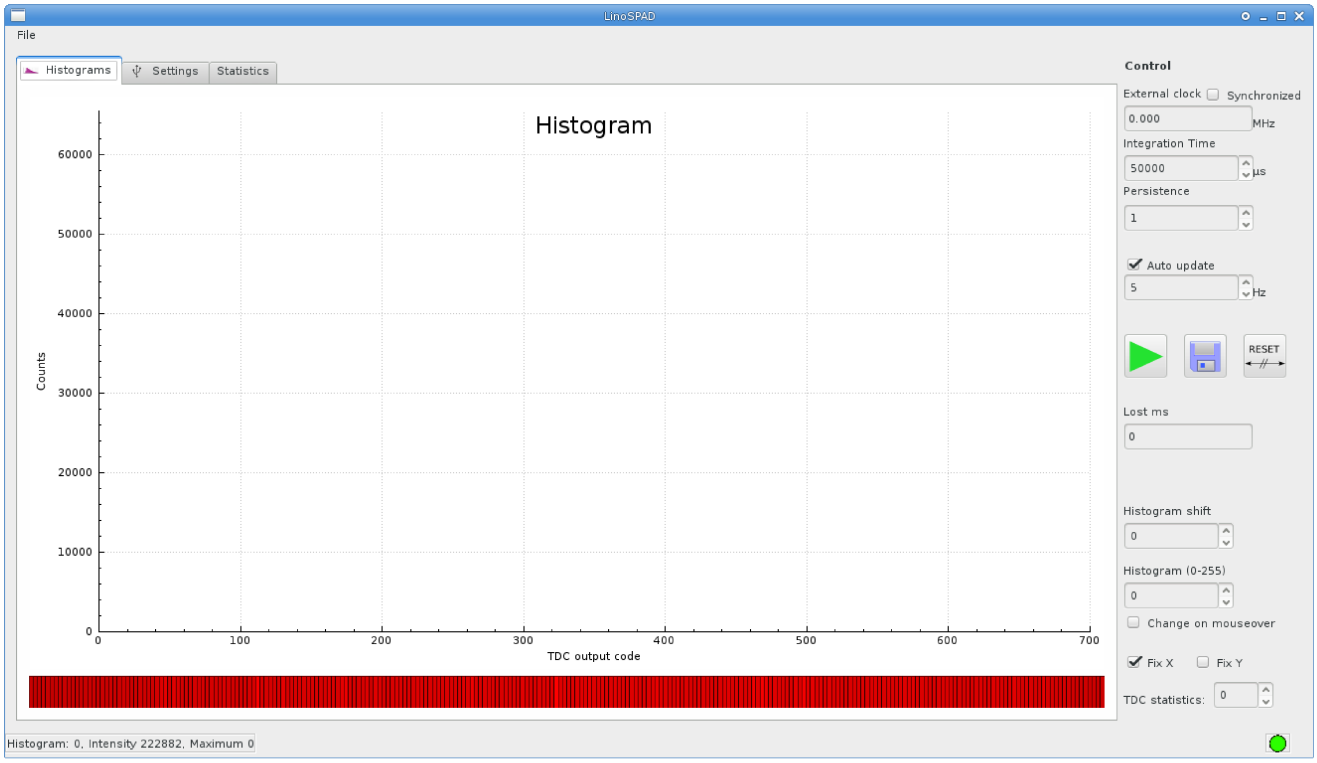
Photon event are accumulated in histograms referenced to an external signal. The firmware can transmit up to 200k histograms of 1024x16bit per second (400 MB/s) though generally a data-rate about 200 MB/s is sustained permanently given that the computer can handle the data. The histograms can be processed during readout to reduce non-linearity from the FPGA delay line implementation.

For the reference signal any signal recognized by the FPGA can be used or it can be generated by the FPGA. The standard firmware supports frequencies of 20, 25, 33, 40, 50, 66, 80 and 100 MHz.



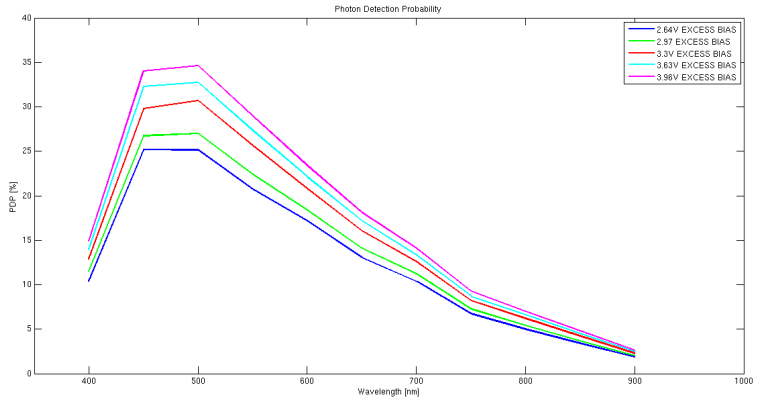
Standard firmware schematic

Software:

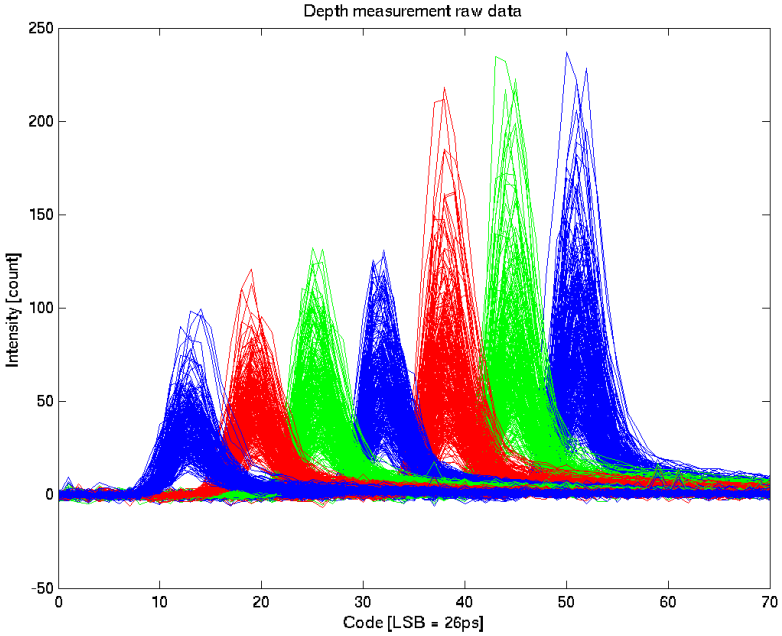


Sensor GUI using QT

Performance:



Photon detection probability versus wavelength for different excess bias voltages.



Sensor data (after FPGA filter) for time-of-flight with a reflective target.