LinoSPAD User Manual

This manual aims to give an overview of the LinoSPAD software and the operation of the camera. After a general introduction on the system architecture and the TDC functionality the different settings in the screen tabs are covered.

General software operation

LinoSPAD is controlled by a computer software that communicates with the FPGA firmware over USB. The communication is handled by a Cypress FX3 USB transceiver that provides a bidirectional stream of 32-bit words between FPGA and computer.

In this communication the computer is always the master that sends commands to the FPGA to which the firmware responds. It is important that the software running on the computer and the firmware in the FPGA 'stay synchronized'. The software expects the firmware to be in a certain state and to receive a certain amount of data as requested from the firmware. When USB timeouts or bad link quality (especially for USB3) cause transfers to fail the software and firmware fall 'out of synchronization' and the system must be reset. The LinoSPAD should be power cycled for this.

The software stores its settings including post-processing and clock synchronization state in a text file in the current directory from where it is loaded when the software starts again.

TDC operation

The firmware contains 64 TDC modules, each shared by 4 pixels. Pixels n, n+64, n+128 and n+192 for n between 0 and 63 share the same TDC. A multiplexer selects which pixel to connect to the delay line.

The delay line is the core of a TDC module. A delay line is constructed from 35 carry elements of 4 bits each in the FPGA logic fabric. The length of the carry chain is thus 140 bits for a delay of at least 2.5ns. Under nominal conditions the line is sampled with 400MHz and generates a code between from 0 to 139 every 2.5ns. Codes corresponding to events from the sensor are handled by the processing logic.

The firmware was initially designed to measure arrival time histograms relative to reference frequencies between 20 and 100MHz. To do this the processing logic contains coarse counters to keep track of the 4 to 20 samples of 2.5ns covering the reference period between 10 and 50ns. The zero reference in the histogram is given by a clock running at the reference frequency synchronous to the 400MHz sampling clock.

The standard histogram has then a raw resolution between 560 (4x140) bins at 100MHz reference frequency and 2800 (20x140) bins at 20MHz reference frequency. The position of the histogram zero

relative to the reference clock edge is given by FPGA routing delays from the input pads to the delay lines and is different for each pixel.

Clock synchronization

All TDC timestamps and resulting histograms are relative to the reference clock used in the system. Clock synchronization between the FPGA and the illumination source is thus of utmost importance to acquire meaningful timing data. Clock synchronization is controlled using the 'Reference clock' tab in the software shown in Figure 1.

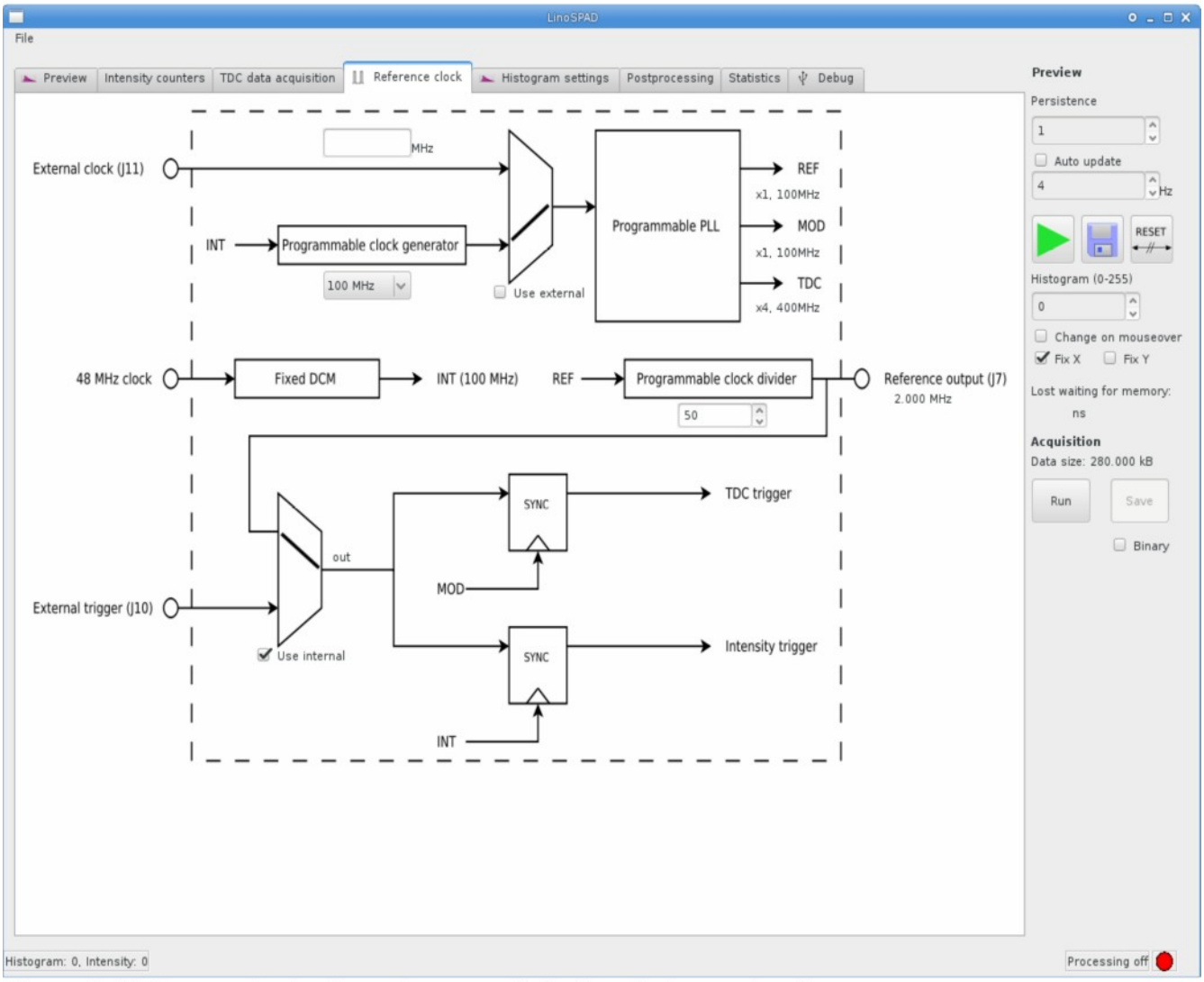

Figure 1: Reference clock tab used to control clock and trigger signals.

All timing is synchronous to the clock named 'REF' coming out of the PLL. This clock is the same as the PLL input clock.

The camera can be operated as master for the illumination by using the internal clock generator and the reference output at J7. In this case the reference clock can be selected between 20 and 100MHz and the reference output can optionally be divided by a even divider. (Valid dividers 1,2,4,6,...,2^17) J7 drives a 2.5V CMOS clock with 50% duty cycle.

When operating the camera as slave to the illumination clock it needs an input clock at one of the available internal frequencies between 20 to 100MHz. The clock need not be the same as the illumination but must be synchronous. To use an external clock connect it to J11 and when the FPGA detects the signal it will show the measured frequency. If the frequency is within range the exclamation mark disappears and the PLL should be able to lock on the signal. The clock source can then be switched by clicking the multiplexer or the tick next to it. The reference voltage for J11 is selected by J3 between 1.8 and 3.3V.

When the illumination source is slower than the reference clock and timestamps or histograms with a longer reference are desired an additional trigger can be used. This trigger can be connected externally on J10. It is synchronized in the FPGA with a clock synchronous to the reference and can be used as zero reference for timestamps and histograms.

Histogram construction

The defining point for the histogram (and timestamps) is the reference signal used to mark the zero. It can be either directly the main clock (REF) or it can be the TDC trigger shown in the 'Reference clock' tab. This selection is done in the 'Histogram settings' tab shown in Figure 2.

When REF is selected the resulting histogram length in bins is shown next to the image. The tick 'Compress histogram 4:1' sums 4 adjacent bins into 0 by discarding the two least significant bits of the timestamp.

For histograms that do not fit into the memory of 1024 bins maximum a code offset can be selected to move the memory window and select alternative portions of the histogram to be stored. Finally the number of items to read from the histogram should be equal to the length of the histogram or the window of interest. When reading timestamps by selecting 'Timestamps' as 'Memory mode' the number of items should probably be 512.

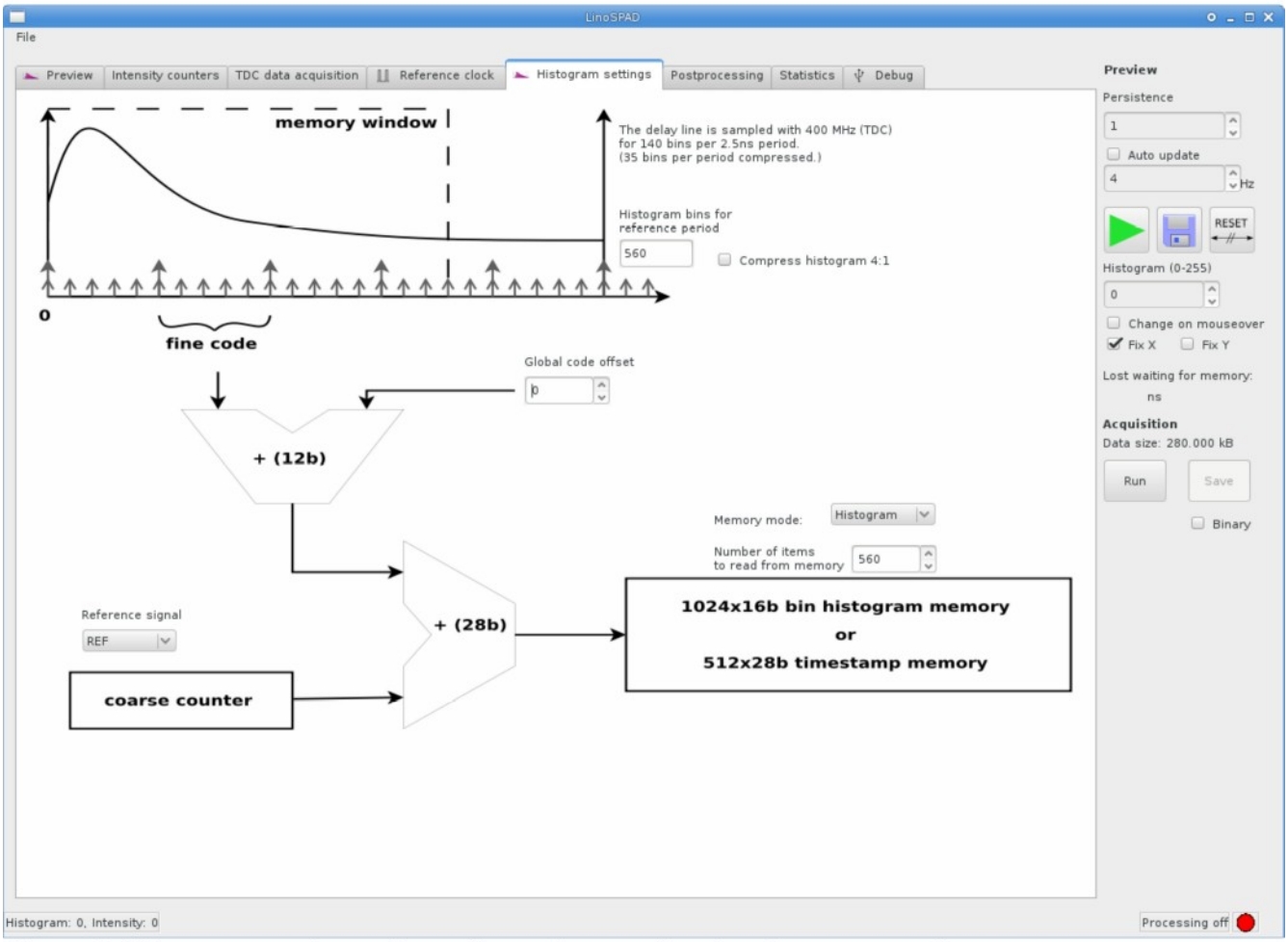

Figure 2: Histogram settings tab to select reference signal and memory mode.

Acquiring data

By default a time-of-arrival-histogram is acquired by summing event timestamps (relative to the reference signal) for a certain time. The 'TDC data acquisition' tab shown in Figure 3 is used to define the length and starting time of the acquisition window.

In addition to the window length the window position relative to the trigger signal can be chosen by enabling 'Wait for trigger' . To acquire a series of histograms the 'Number of acquisition cycles' can be set higher than its default '4'. The default value cycles over the four sets of pixels acquiring a histogram for each pixel. This operation is also executed when using the preview functionality.

The ticks and buttons for multiplexer and memory operation can at this point be used to acquire over a series of windows synchronous to a slow reference. (Disabling all ticks leads to a number of windows equal to the number of cycles. After acquisition the data is received by clicking 'Switch buffers' followed by 'Read back buffer'.) It is planned to extend this functionality in the future. Contact us if

you need more information.

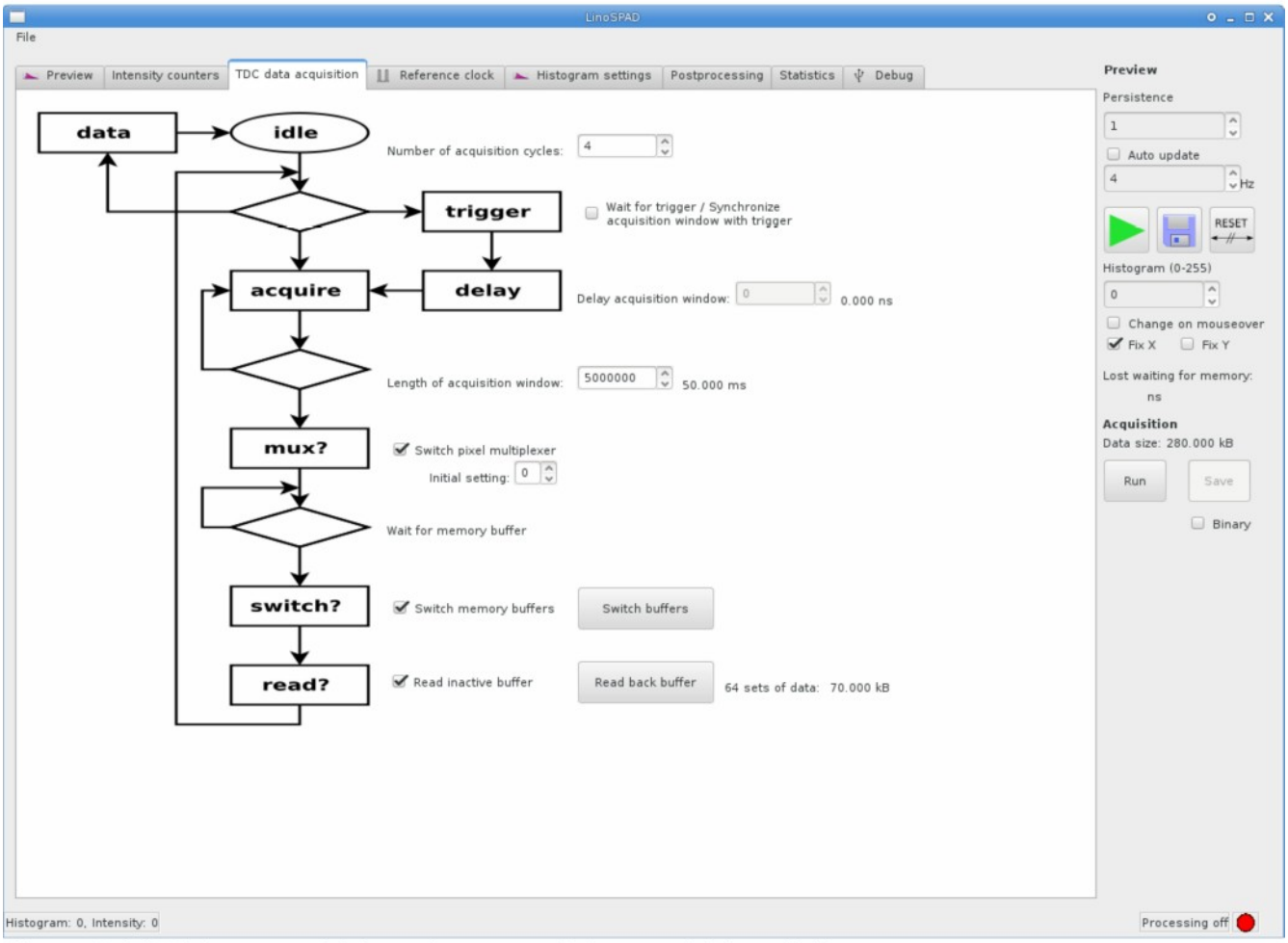

Figure 3: TDC data acquisition tab to control the acquisition window.

To run an acquisition of more than 4 cycles the buttons on the right under 'Acquisition' are used.

Data Preview

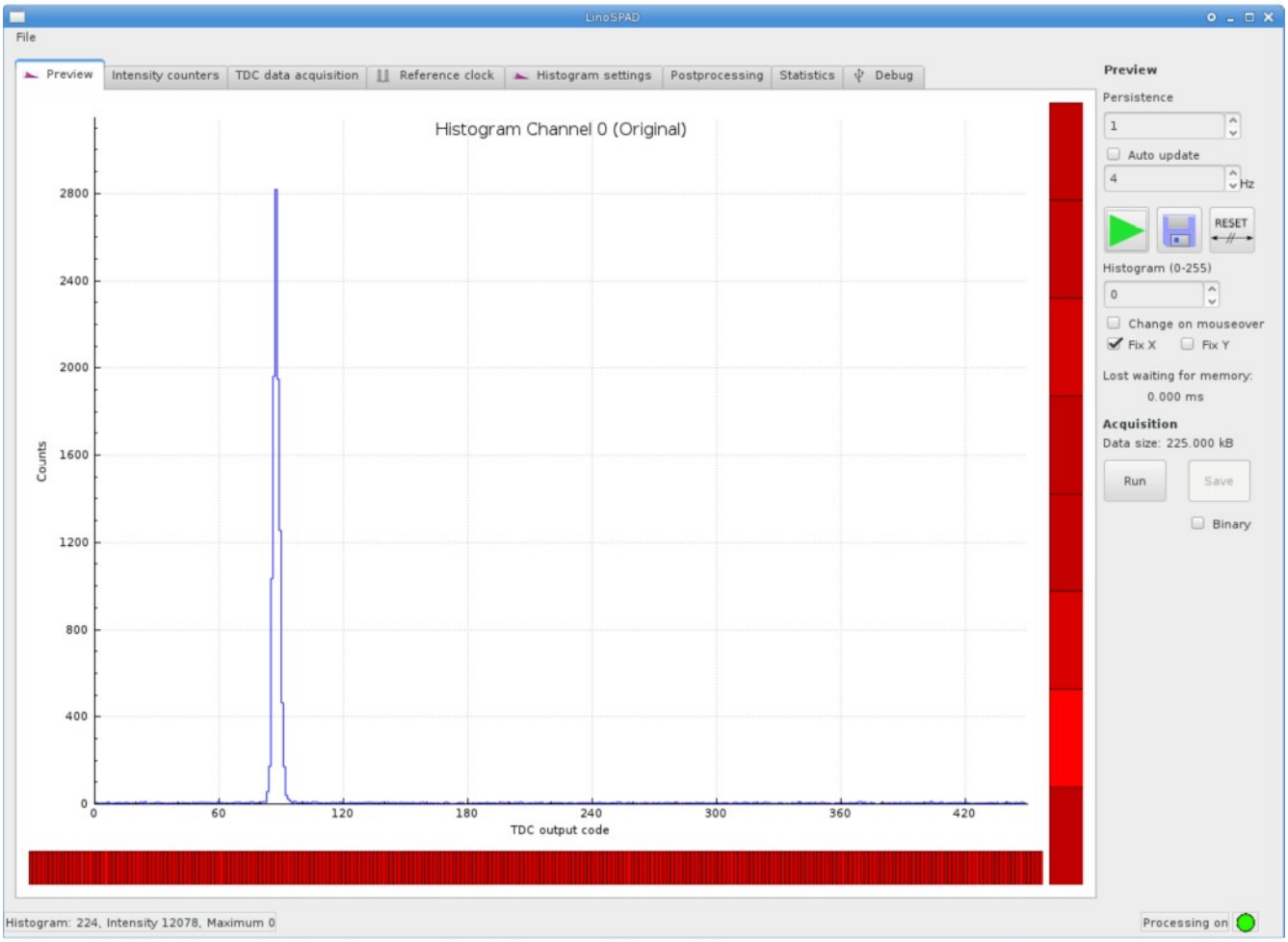

Figure 4: Preview tab showing received data and intensities.

The 'Preview' tab shown in Figure 4 is used to display the data received from the camera. The central graph can be grabbed with the mouse to pan the area and the mouse-wheel can be used for zoom. The X and Y axes can be individually fixed using the ticks on the right. The selected histogram is equally selected on the right. It can be switched using up and down cursors.

The red bars on the bottom and to the right of the data graph show the pixel intensities read from the camera using the intensity counters. In auto-updating mode the intensity is computed from the histograms.

A click on the green arrow (or a press of Enter) acquires one set of histograms (one for each pixel) by running 4 cycles of data acquisition. When auto-update is enabled the preview is further updated with the frequency chosen. The 'Persistence' control enables an averaging of the display over multiple acquisitions.

The on-screen data can be saved using the middle disk button and graph axes can be reset using the right-most button. Enabling 'Change on mousover' makes the histogram switch to the pixel pointed at in the horizontal intensity bar.

Postprocessing

On its way from the FPGA memory to the computer histogram data can be post-processed to smooth non-linearities inherent in the delay chains.

To use the postprocessing functionality a sufficient amount of raw (unprocessed) data needs to be collected to be analyzed by the software. When postprocessing is disabled all previewed histograms will be summed up for this purpose. The number of summed up histograms is visible in the 'Postprocessing' tab shown in Figure 5. A click on 'Reset' discards old data after changes to the other settings.

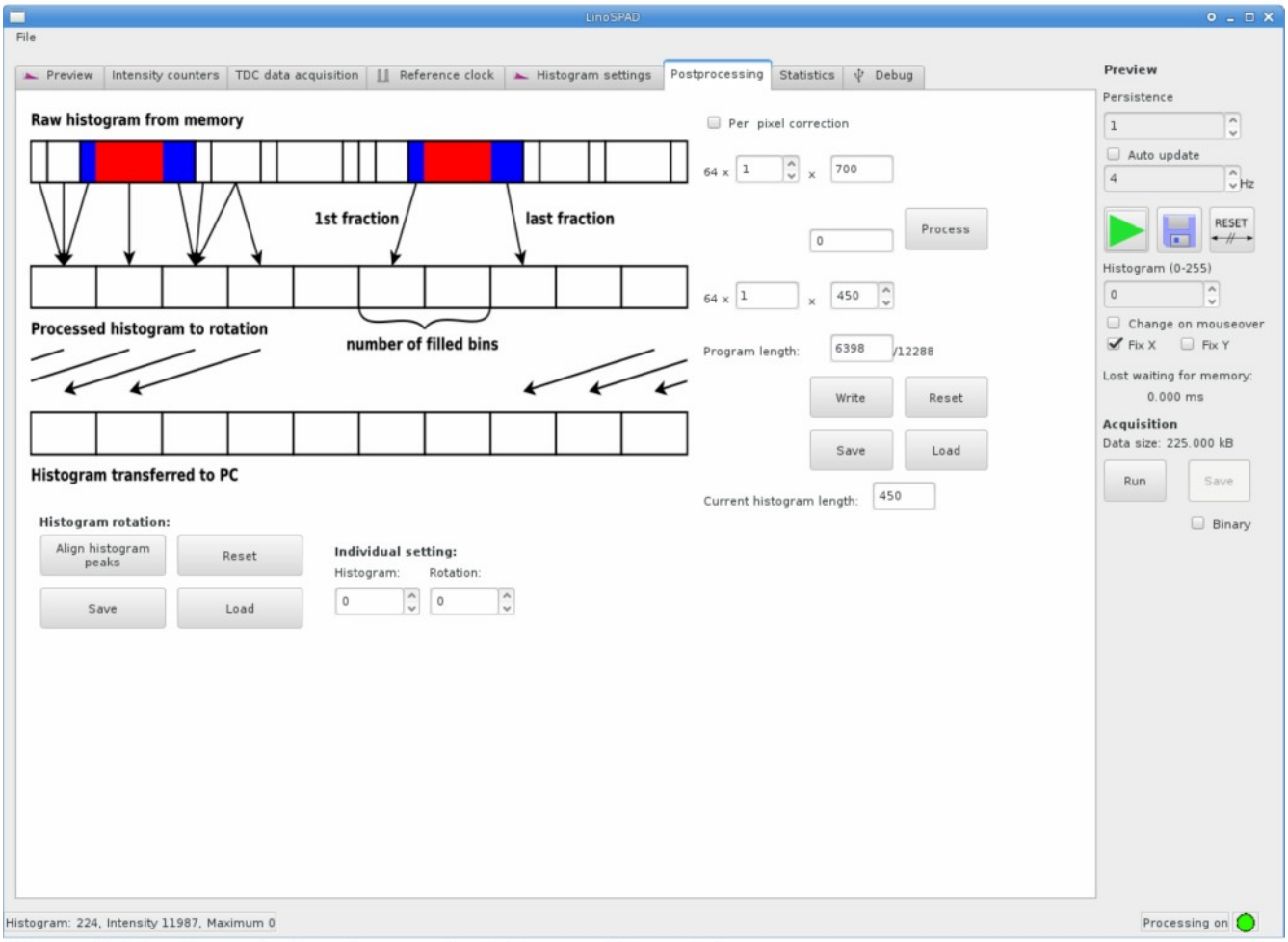

Figure 5: Preview tab showing received data and intensities.

Once enough data has been collected it can then be processed by clicking the button. This will analyze

the statistical distribution of the events over the histogram bins and compute correction factors to create a uniform histogram of chosen length. When the process is successful the resulting correction program length is shown and TDC statistics are available in the 'Statistics' tab.

The statistics (and program) can be saved and loaded in the software and written to the FPGA using the respective buttons.

The zero reference of histograms of different pixels is not aligned due to the delays in the FPGA from the input to the delay line not being matched. The histogram rotation can be used to rotate short histograms such that the bins become aligned. Individual histograms can be rotated using the spin controls. 'Align histogram peaks' uses the on-screen (smoothed) data and rotates the maximum bins to the middle of the histograms.

Intensity counters & Debug tabs

The 'Intensity counters' tab gives access to the main intensity counters shown in the bottom bar of the 'Preview' tab. Each pixel connects to two 32bit counters sampled at 100MHz. The first counter increments when the pixel is sampled high, the second increments when an edge is detected.

Keyboard controls

The following keyboard-shortcuts are defined:

- Up/Down arrow – Switch displayed histogram
- Enter – Start/Stop preview
- CTRL + S – Save preview
- Escape – Close program
- (Shift) Tab – Cycle tabs

File formats

Data is stored in text format by default. Histograms are written one pixel after the other, one value per line. All setting files are text format as well.

Timestamp mode

Timestamp mode is enabled by switching the 'Memory mode' in the 'Histogram settings' tab. In this mode the system records timestamps in the memory usually used to store histograms. The length of the histogram corresponds to the highest occurring timestamp. The timestamps have a resolution of 28bit such that only 512 can be stored per TDC. Valid timestamps have the highest bit set (2^31 added) when saved after acquisition to indicate cases where not all TDCs generated enough timestamps. Saved previews store zero in these positions.

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